68002

Total No. of Questions : 6 Total No. of Printed Pages : 4

EIS-29

B.E. (VIth Sem.) (CGPA) (El & Comm. Engg.) Exam.-2015

VLSI DESIGN

Paper : EL-604

Time Allowed : Three Hours
Maximum Marks : 60

Note : Attempt all questions.
There is internal choice in the questions.
All questions carry equal marks.

Q.I Define the following terms— 10

(a) Sequence detector

(b) Multivalued logic in VHDL

(c) PLA

(d) Operator overloading in VHDL

(e) VSART

Q.II (a) Design a mealy sequential machine which converts 8.4.2.1 BCD code to excess-3 code realize the design using D flipflop. 7

(b) Implement the design of a substractor (3bit) using NOR gates. 3

or

(a) Write a VHDL function that will take the 2's complement of a n bit vector. Use a call of the form comp2 (bit-Vec, N), Where N is the length of the vector. 5

(b) Discuss variable, signal and constant assignment used in VHDL with example. 5

Q.III (a) Write VHDL description of a 4bit up/down synchronous counter with output Q. All state changes occur on the rising edge of the clock input other inputs are load (to load the count) CLR (to reset output) and Enable (to start counting. 6

(b) Explain simulation and synthesis process. 4

or

(a) Write VHDL description for 8 bit parallel adder using single bit adder as component. Use generate statement. 5

(b) Describe attributes, signal resolution and generics used in VHDL. 5

Q.IV (a) Implement a 4 x 16 decoder using ROM. 5

(b) Classify programmable logic devices and compare them. 5

or

(a) Draw and explain the generalized block diagram of FPGA. What is a LLB ? Explain. 5

(b) Draw the flow chart of floating point multiplication and explain it with suitable example. 5

Q.V (a) Describe the basic boundary scan architecture with diagram. 5

(b) Draw the block diagram of 4-bit BILBO register and write its VHDL code. 5

or

Discuss combinational logic testing and explain with suitable example stuck-at 0 and stuck at -1 fault and how it can be overcome.

Q.VI (a) Draw the parallel port block diagram and write VHDL code for the parallel port of a micro controller. 7

(b) Explain the need of transport and inertial delay. 3

or

(a) Draw the block diagram of USART and give VHDL description for its interfacing with microprocessor. 5

(b) Write VHDL function to determine HCF of an array of integers. 5

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