

Total No. of Questions : 6

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B.E. VIth Semester Examination, 2014

Electronics

VLSI Design

Paper - EL-604

Time : 3 Hours]

[Maximum Marks : 60]

Note :- Attempt all questions.

✓ Answer the following questions in short : $5 \times 2 = 10$

- (i) What are hazards in combinational circuits?
 - (ii) Define Setup & hold time for a DFF.
 - (iii) Name the type of delays provided by VHDL.
 - (iv) What is TEXT I/O package in VHDL?
 - (v) What is operator overloading?
2. (a) A synchronous sequential network has one input and one output. If the input sequence 0101 or 0110 occurs,

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curs, an output of two successive 1's will occur. The first of these μ should occur coincident with the last input of the 0101 or 0110 sequence. The network should reset when the second 1 output occurs. Derive mealy state table and diagram and implement it using JKFF.

- (b) Define and compare Mealy and Moore machines. 3

OR

- (a) Write VHDL code for a 4 bit subtractor using single bit substrator as a component using structural modeling.

- (b) Write VHDL description for a 4 bit up/down counter (synchronous). The code should contain a statement of the form "Process (Down, Up, CLR, Load)"

3. (a) Discuss IEEE 1164 standard logic and signal resolution.
 (b) Write VHDL test bench for functional simulation of a 3×3 decoder circuit.

OR

- (a) Explain Generics in brief. Write a VHDL code of generic N-input And gate.

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- (b) Write a VHDL model using Generate statement for an 8 bit comparator.
4. (a) Find a Minimum row PLA table to implement the following function :-

$$f_1(A_i B_i C_i D) = \Sigma m(4, 5, 10, 11, 12)$$

$$f_2(A_i B_i C_i D) = \Sigma m(0, 1, 3, 4, 8, 11)$$

$$f_3(A_i B_i C_i D) = \Sigma m(0, 4, 10, 12, 14)$$

- (b) The following state table is implemented using a ROM and two D flipflops.

Q, Q ₁	Q ₀ ' Q ₁ '		Z	
	x=0	x=1	x=0	x=1
00	01	10	0	1
01	10	00	1	1
10	00	01	1	0

Draw the Block diagram

OR

- (a) Discuss the architecture of FPGA

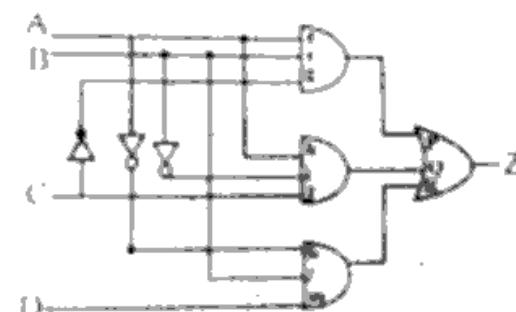
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- (b) Discuss floating point multiplication using flow chart.

5. (a) For the following network, find a minimum number of test vectors that will test all s-a-0 and s-a-1 faults at the AND and or gate inputs



- (b) Discuss Basic boundary Scan architecture.

OR

- (a) Discuss MISR and BILBO registers used in BIST.
- (b) Explain the advantage of using configurations. Show how a full adder can be modeled in different ways using configuration.

6. (a) Discuss the block diagram of Parallel port used in a microcontroller and write VHDL code for it.

- (b) Discuss signal and variable assignment in VHDL. 4

OR

- (a) Draw the design flow chart of VART transmitter and give its Entity declaration in VHDL.
- (b) Discuss function & procedure commands used in VHDL.

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